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Design of Continuous Time Sigma Delta ADC for Signal Processing Application

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Abstract— *This paper attempts an accurate design of low power Voltage Controlled Oscillator (VCO) enabled quantizer in Continuous Time Sigma Delta ADC in 180nm CMOS technology using Tanner EDA tools. The architecture of the method consists of a loop filter, VCO quantizer and the DAC in the feedback side of model. The Operational Amplifier (OPAMP) is used in design of loop filters which offers 40.1dB gain, 70 degree phase margin and unity gain bandwidth of 79.06MHz. Even order harmonics of VCO are reduced by VCO quantizer loop structures. The Higher order loop filter is designed using an active Resistance and Capacitive based integrators and VCO quantizer is implemented using 15 multiple stage ring oscillator and register of DFF. This provides a benefit of low phase noise with frequency of 100 MHz rang. The power dissipation of overall circuit is very satisfacory 3.5 mW.*

Keywords— *Analog to Digital Converter (ADC), Operational Amplifier (OPAMP), nonidealities, Voltage Controlled Oscillator (VCO).*

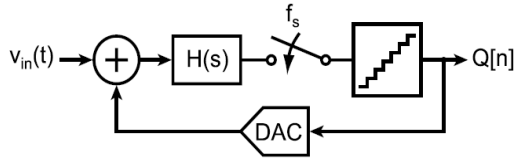
1. INTRODUCTION

Integrated circuit (IC) technology result in many advances in implementation of digital logic on silicon which moved many types of signal processing to the digital domain[1-5]. One of the important applications of this phenomenon is in data converters: Digital to Analog converters (DACs), Analog to Digital Converters (ADCs) and now Continuous Time ∑Δ ADC structures are also implemented. A promising ADC structure called Continuous Time ∑Δ ADC structures has become current topic of research that claims to provide excellent power efficiency [5]. The major role to perform analog to digital conversion with significantly relaxed matching requirements on analog components[6-9].

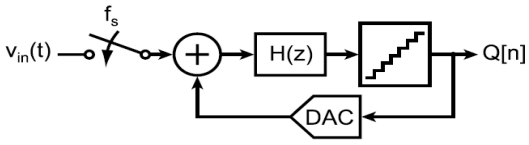
Conventional analog Continuous time ∑Δ ADC includes a comparator circuit having high speed and low noise in the loop as the quantizer and hence it poses a design challenge in deep submicron technology. The design of ADCs is difficult due to the low supply voltage due to the technology scaling and it require complex analog buildings blocks [8]. While a Voltage Controlled Oscillator (VCO) based quantization is realized in a CMOS technology easily and this can be used for high speed applications also [10-14]. This quantization has become interesting research topic due to its unique and attractive signal processing features. There are various methods to deal with the distortion caused by the VCO's nonlinear tuning curve. VCO based ADC's employ digital circuits that results in technology scaling. Continuous time ∑Δ ADC are also hot topic for research used in numerous applications such as radio, wireless receiver, audio, communication etc [14].

1.1 A Brief Overview of ∑Δ ADC

The basic prpoperty of the CT ∑Δ ADC is its inherent anti-alias filtering ability that allows input analog signal which is first applied to CT loop filter before sampling by the VCO quantizer as can be seen Fig.1.(a), whereas in DT ∑Δ ADC samples the input analog signal before it applied to loop filter as shown in Fig.1.(b). The same is also true for any other DT ADC (SAR, pipeline, flash, etc) as sampling always happens before the input of ADC.



(a)



(b)

Fig. 1: Sampler (a) CT ∑Δ ADC (b) DT ∑Δ ADC

The inherent anti-alias filtering ability of the CT ∑Δ ADC's is used as a means to simplify baseband filtering and digitization in wireless systems. However, CT ∑Δ ADC could be clocked up to an order of magnitude faster in the same technology without much performance penalty.

Unfortunately designing an anti-alias filter introduces distortion and minimal noise that takes area consumption

and high power dissipation. The power dissipation varies from 10mW to 100mW or more that depends on how much noise signal is there; linearity and bandwidth. The design parameters of CT ∑Δ ADC are shown in Table.1

2. SYSTEM ARCHITECTURES

The architecture of VCO based CT ∑Δ ADC is shown in Fig 2. Loop filter provides noise shaping and linearity is improved. The quantization noise is also reduced with good power efficient characteristics. The VCO converts the analog input voltage into an output frequency which is a linear function of input voltage. VCO based ADC is used that allows high speed of operation with small latency.

In the DAC design normally, each phase output is connected to one DAC cell and added together to obtain the feedback signal. The NRZ and RZ DAC both act as feedback connected to VCO quantizer for achieving monotonicity.

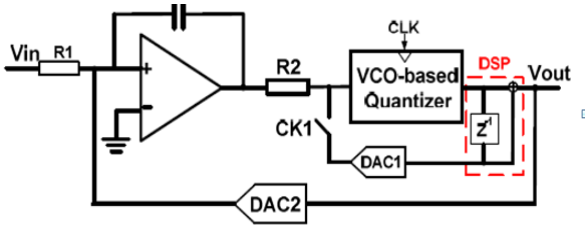


Fig. 2: Proposed VCO quantizer based CT ∑Δ ADC.

The CT ∑Δ ADC's has concerns related to the high sensitivity to clock jitter due to modulation of DAC charge that appears at ADC input as shown in Fig. 3. The RZ DAC was tested and more jitter sensitivity was found as compared to NRZ DAC.

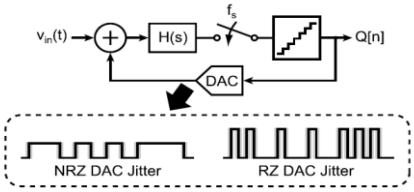


Fig. 3: Clock jitters in a 1-bit NRZ and RZ feedback DAC

The SNR degradation takes place due to clock jitter which can be reduced by a Multibit quantize rand NRZ with feedback DAC implementation[5,10]. Fig. 4 shows that jitter modulates the DAC charges of the LSB's that change from sample to sample. The bits increase then error is reduced. Mixed signal designs of CT ∑Δ ADC will have other challenges: high resolution, bandwidth and power efficiency and deep sub-micron technologies[3].

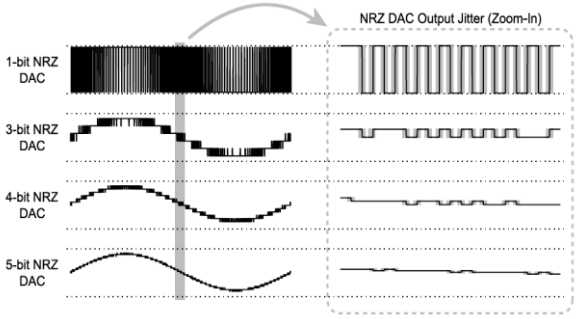


Fig. 4: Increasing the number of bits in a Multibit NRZ DAC reduces the error charge modulation.

3. PROPOSED CONTINUOUS-TIME ΣΔ ADC TOPOLOGY

A prototype VCO quantizer based CT ∑Δ ADC is designed with reduced nonlinearity. The building blocks of loop filter, VCO quantizer and DAC are designed with thick oxide devices operating at 2.5V and 1.8V. The proposed architecture of VCO based CT ∑Δ ADC is shown in Fig.5.

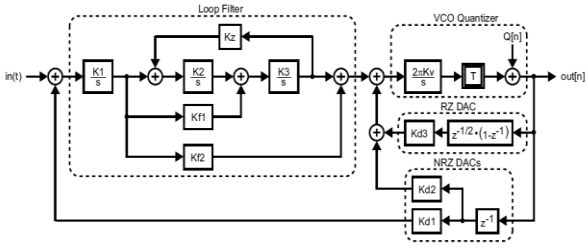


Fig. 5: Proposed Loop filter with VCO quantizer and feedback DAC.

3.1 Loop Filter

The loop filter of ∑Δ ADC has noise-shaping property which suppresses the VCO nonlinearity to the extent of its gain in the signal bandwidth. Higher order noise shaping can be achieved by increasing the order of loop filter. The filter order of four is realized using an active RC integrator as shown in Fig. 6. There are three different types of topology used: Active RC, Gm-C and MOSFET-C integrator.

Active RC integrators have better linearity and larger signal swing and hence the active RC topology is chosen for its excellent linearity. The amplifier in the integrator is implemented two-stage OPAMP. The first stage is differential stage and the second stage is implemented with the common source. The feed forward path from the input to second stage is implemented as shown in Fig.7. The effectiveness of the method depends on the gain of the loop filter, because VCO quantizer input scans the

entire signal range and it exercises the entire nonlinear tuning curve of VCO. As a consequence, high gain loop filter suppresses the large amount of distortion caused by the VCO affecting the ADC performance. The simulated result of two-stage OPAMP with tanner EDA tool with 0.18um CMOS technology is shown in Fig. 8. The design requirement of two-stage OPAMP is phase margin of 60^0 or more to get high stability. The OPAMP achieves a DC gain, phase margin and unity gain bandwidth of 40dB, 70^o and 79.06MHz respectively with power (V_{DD}) 1.8V.

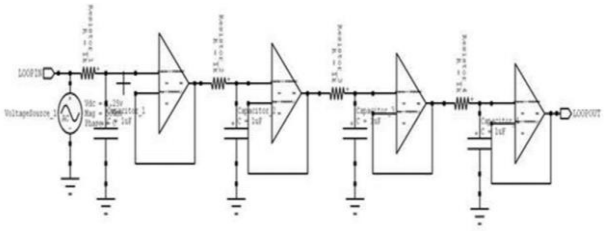


Fig. 6: Fourth order loop filter using two stage OPAMP

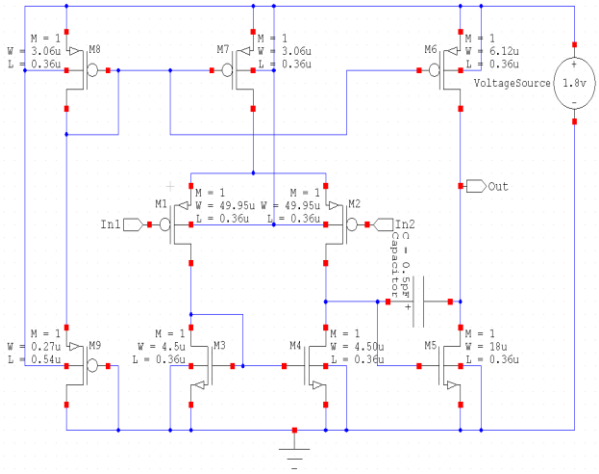


Fig. 7: Two stage OPAMP using CMOS Realization

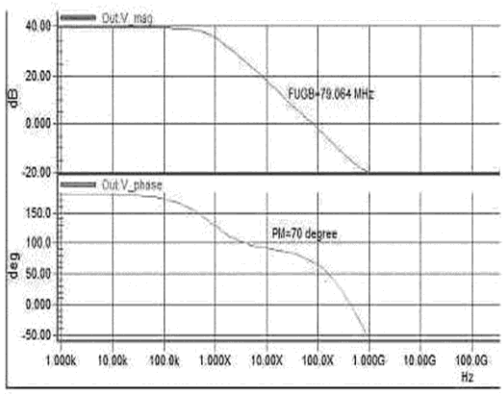


Fig. 8: Simulated magnitude and phase response of OPAMP

3.2 VCO Quantizer

VCO based quantizer converts analog input signal in to digital data and produces a continuous time based signal whose frequency is directly proportional to the average analog input signal. Resolution depends on the number of phases of VCO. There are two main types of architectures for VCO based ADCs namely counter based architecture and phase detector based architecture. VCO used in VCO-based ADC suffers from high non-linearity, considering that a differential structure and non-ideal effects can be inherently reduced.

VCO quantizer consists of multistage ring oscillator (RO), two arrays of DFFs and an array of XOR as shown in Fig. 9. The DFFs prevent the previous phase states of VCO. The XOR gate compares the DFFs and determines whether the VCO undergoes a transition. The final output is equal to the number of elements under transition which is controlled by control voltage of the VCO. The VCO quantizer is simulated in 0.18um CMOS techniques with the frequency 100 KHz with the input voltage and offset of amplitude 1.25V as shown in Fig.10. The power consumption is 3.8mW.

3.3 Feedback DAC

The most important component of feedback path is the 1 bit DAC which converts the output digital streams to analog signal. A sigma delta convertor uses multi bit quantizer and multibit digital-to-analog (DAC) to reconstruct the analog signal, for such DAC the linearity of the convertor is important. For a high resolution DAC,

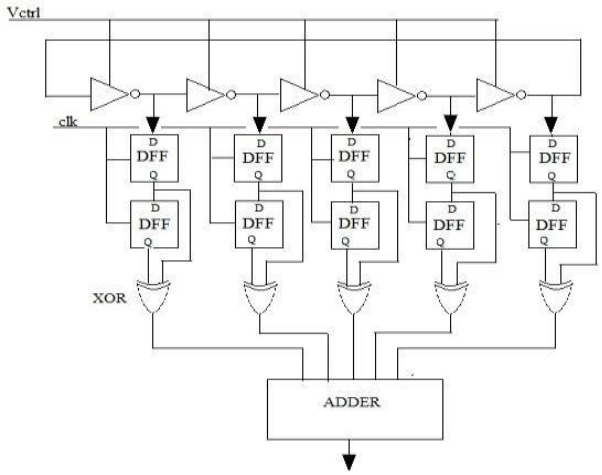


Fig. 9: VCO quantizer based on multistage ring oscillator with the arrays of DFFs and XOR

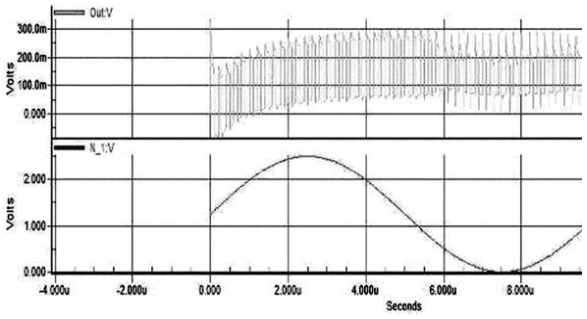


Fig. 10: Output of the proposed VCO quantizer

accuracy is one of the major problems. In one bit DAC, linearity is determined by the accuracy of switching between the references signals, for high switching accuracy the system will be linear.

4. EXPERIMENTAL RESULTS

A Sigma delta Analog to digital Convertor is designed by integrating the components of the system in 0.18um CMOS technology using Tanner EDA tool. OPAMP which is one of the key components has an open loop gain of 40dB and a phase margin of 70^0, which helps smooth operation of the integrator circuit. A high speed VCO quantizer is designed using 15-stage Ring oscillator with arrays of DFFs and XOR. The proposed VCO quantizer is implemented at 100 KHz sampling frequency and amplitude of 1.25V with low power dissipation of 3.8mW and hence gives the corresponding result which is then fed to 1 bit Digital to Analog (DAC) circuit at the feedback path of the system. This process is iterated and a pulse of digital signal is achieved at the output of the system. The performance of VCO based architectures is summarized in Table 1. We present a comparison chart between VCO power and different technologies which give quick orientation as shown in Fig. 11.

Table 1: Performance Comparsion with Previous works

Ref.	*Techno-logy (nm)*	*Operating frequency of VCO (MHz)*	*VCO Power (mW)*	*Gain (dB)*	*Supply voltage (V)*
[1]	a. 180	b. 2.5	-	c. -	d. 1.8
[6]	e. 90	f. 0.1-4	g. 1.3	h. 58	i. -
[9]	j. 130	k. 225	l. 18	m. 63	n. 1.5
[10]	o. 130	p. 10	q. 20	r. 50	s. 1.2
[11]	130	t. 640	u. 20/18	v. -	w. 1.2
[14]	x. 180	y. 100	z. 3.8	aa. 40	bb. 1.8
This work	cc. 180	dd. 100	ee. 3.5	ff. 40.1	gg. 1.8

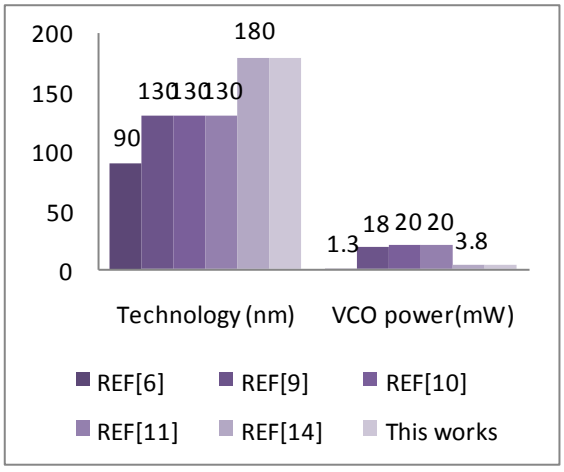


Fig. 11: Comparison chart of various results

5. CONCLUSION

It has been observed that high performance low power VCO-based sigma delta ADC architecture is accurately designed in nanometer scale range of the CMOS technology. The amount of distortion is reduced by gain of 40 dB of the loop filter and hence the VCO nonlinearity is improved. The order of noise rejection is highly improved and linearity at 100 KHz frequency becomes better. Computed power consumption which is 3.8 milliwatts using VCO enabled quantizer in 180 nm CMOS technology**.**

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